AMENDMENTS TO THE SPECIFICATION

Amend paragraphs [31] and [32] in the Brief Description of the Drawings section as follows:

[31] FIG. 12 illustrates the temperature dependence of the DC voltage generator for different sampling frequencies; ~~and~~

[32] FIG. 13 illustrates the use of frequency compensation to make the DC voltage generator insensitive to temperature variation~~s~~ ; and

Add the following new paragraph [32.1].

[32.1] FIG. 14 illustrates a linear feedback shift register that may be used for the bit-stream generator of FIG. 1.

Amend paragraph [39] in the Detailed Description of the Invention section as follows:

[39] Many alternative digital pulse modulation generators 12 are envisioned within the present invention. For example, yet another memory based manner of generating a periodic bit-stream that is simple and compact to implement and an alternative to the D flip-flops of ~~Fig.~~ FIG. 1 is a linear feedback shift register (LFSR) ~~(not shown)~~, such as LSFR 15 of FIG. 14. If only limited flexibility is required (in terms of the number of DC levels that need by encoded), ~~a~~ an LSFR is a viable implementation for generating the periodic sequence fed to averaging circuit 14.

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